REMARKS

A. Status of the Claims

Claims 1 and 2 are pending in the application. Claims 1 and 2 were rejected under 35 USC 103(a) as being unpatentable over Mohsen et al., US Patent No. 4,881,114, in view of Zhang, US Patent No. 5,835,396. Claim 1 was rejected under 35 USC 103(a) as being unpatentable over Zhang in view of Takagi et al., US Patent No. 5,866,938. Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Zhang in view of Takagi et al. and further in view of Ohmi et al., US Patent No. 5,714,795.

B. 35 USC 103(a) Rejection: Mohsen and Zhang; Claims 1 and 2

Claims 1 and 2 were rejected under 35 USC 103(a) as being unpatentable over Mohsen et al. in view of Zhang.

Claim 1 recites a three dimensional multi-level memory array disposed above a substrate, the array comprising a plurality of memory cells, each memory cell comprising a silicon nitride antifuse.

The Examiner points to the device of Mohsen et al., which includes (in Fig. 1), a first moderately doped layer 12 formed in a semiconductor substrate 10, an antifuse layer 14 which may be silicon nitride, and a second heavily doped silicon layer 16 of a conductivity type opposite the first (col. 3, lines 42-64 and col. 4, lines 21-25.)

The Examiner asserts:

> Zhang discloses three dimensional multi-level memory arrays having units substantially similar to that of Mohsen ... It would have been obvious to one of ordinary skill in the art ... to modify the memory cell array of Mohsen, such that it is formed in a three dimensional, multilevel array, as suggested by Zhang ...

Applicants respectfully point out, however, that the memory cell of Mohsen et al. cannot be formed in a three dimensional, multilevel array like the one described by Zhang without fundamentally changing its character, mode of fabrication, and function.

Layer 12 of the device of Mohsen is formed in substrate 10, which those skilled in the art would assume to be a monocrystalline silicon wafer, as in the example in Mohsen et al. (col. 7, line 56 *et seq.*) Thus at least one part of the diode of Mohsen et al. comprises monocrystalline silicon. The "quasi-conduction layer" of Zhang, however, is taught to be amorphous or polycrystalline silicon (col. 6, lines 50-54.) The use of amorphous or polycrystalline silicon in the devices of Zhang cannot be considered a mere design choice. The quasi-conduction layer of Zhang is formed by depositing silicon above a substrate. Deposited silicon will not be monocrystalline without use of extraordinary measures such as laser recrystallization, which are certainly nowhere suggested in either Mohsen et al. or Zhang.

As is well understood by those skilled in the art, crystallinity of semiconductor material has strong influence on its behavior and on the performance of the device in which it is used. The device of Mohsen et al. cannot be transplanted into the Zhang array without becoming a different device.

Applicants believe the references cannot be successfully combined, and respectfully request reconsideration.

C. 35 USC 103(a) Rejections: Zhang, Takagi, and Ohmi; Claims 1 and 2

Claim 1 was further rejected under 35 USC 103(a) as being unpatentable over Zhang in view of Takagi et al.

The Examiner suggests it would have been obvious to modify the antifuse of Zhang to be silicon nitride:

> ... because Takagi shows that it has high resistivity and a highly selectable breakdown voltage, thus allowing for a stable anti-fuse layer ...

In Zhang the antifuse is in a nonvolatile memory cell, generally adjacent to a quasi-conduction layer, for example of amorphous or polycrystalline silicon (col. 6, lines 50-54.) The device of Takagi et al., however, is a nonstoichiometric silicon nitride layer (col. 6, lines 6-8) disposed between two layers of Ti/TiN (layers 16 and 17, Fig. 2, col. 7, lines 58-61) in an FPGA (col. 7, line 42), an entirely unrelated context with very different requirements.

The Examiner points to col. 2, lines 1-15 of Takagi et al. as evidence that silicon nitride provides the advantages listed in this passage. It is clear, however, that these lines instead describe the characteristics that an antifuse *between conductive layers in an FPGA* should advantageously have (col. 7, lines 58-67.) Takagi et al. then go on to further specify (col. 8, lines 23-40) specific resistances and other characteristics "for the antifuse of FPGA," and ultimately suggest a material, a nonstoichiometric silicon nitride. The teachings of Takagi et al. are clearly focused to formation of an antifuse in an FPGA.

There is no suggestion in Takagi et al., however, that this material, or any other form of silicon nitride, is generally useful in all antifuses found in all devices. The antifuse of Zhang, for example, is not formed between layers of Ti/TiN, but rather adjacent an amorphous or polycrystalline diode. It will face programming conditions entirely unrelated to those of the device of Takagi et al., and must withstand repeated reads without experiencing dielectric rupture. The voltages experienced by the antifuse in an FPGA are crucial to the choice of Takagi et al., but in no way applicable to Zhang.

The doped amorphous or polycrystalline silicon of Zhang will provide a very different current than will the Ti/TiN contacts of Takagi et al. In short, there is no reason to apply the teachings of Takagi et al. to the memory of Zhang.

Applicants suggest, then, that there is no motivation to combine the references, and respectfully request reconsideration.

Claim 2 was further rejected under 35 USC 103(a) as being unpatentable over Zhang in view of Takagi et al. and further in view of Ohmi et al.

Applicants have already explained that no motivation exists to combine the teachings of Zhang and Takagi et al. By the same rationale, Applicants maintain there is no motivation to make the combination of references proposed by the Examiner for this 35 USC 103(a) rejection of claim 2.

Applicants respectfully request reconsideration.

CONCLUSION

In light of this response, Applicants believe this application to be in condition for allowance.

If there are any questions concerning this response, the Examiner is invited to contact the undersigned agent at (408) 869-2921.

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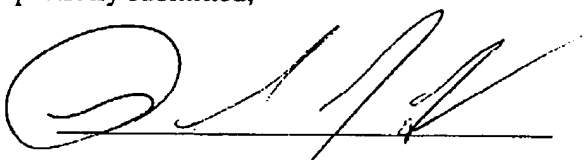
Respectfully submitted,



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